A 1.8-GHz High-Efficiency 34-dBm Silicon Bipolar Power Amplifier

Francesco Carrara, *Student Member, IEEE*, Antonino Scuderi, Tonio Biondi, and Giuseppe Palmisano

***Abstract*—The low-voltage power capabilities of a low-cost high-performance silicon bipolar process were investigated. By optimizing the emitter finger layout, epilayer thickness, and collector doping level, efficiency values up to 83% were achieved by on-wafer load–pull measurements on a single-cell test device operating at 1.8 GHz and 2.7-V power supply. The detrimental effect of the emitter distributed resistance on the current capability of long-emitter bipolar transistors was also considered. An analytical model for a proper device design was derived and experimentally validated. Using the optimized unit power device, a 1.8-GHz 2.7-V three-stage monolithic power amplifier was implemented, which provides a 57% power-added efficiency and a 33-dB gain while delivering a 34-dBm output power to the load.**

***Index Terms*—DC current capability, mobile communications, RF power amplifier (PA), silicon bipolar technology.**

I. Introduction

HIGHLY efficient RF power amplifiers (PAs) are in great demand to enable low power consumption and extend operating time for portable radio equipment. Low-voltage operation is a key design issue as well since reduced battery size allows compact and light handsets to be used. Currently, the PA market is dominated by GaAs-based modules or monolithic microwave integrated circuits (MMICs) since they can provide excellent performance in meeting such requirements. However, cost estimates show that the PA is one of the most expensive components in cellular handsets. Therefore, cost-competitive power devices and manufacturing processes are crucial for high-volume production. As is well known, silicon-based technologies have inherent advantages in the implementation of low-cost RF integrated circuits (RFICs) over III–V semiconductors. For this reason, the prospect of an efficient RF PA in pure silicon technology has been attracting increasing attention over the last few years [1]–[11]. As far as performance is concerned, excellent results have been demonstrated both at 900 MHz [10] and 1.9 GHz [11] by using silicon bipolar devices. A differential approach is proposed in [10] and [11] with integrated transformers and off-chip lumped *L-C* baluns. Moreover, the development of the first silicon bipolar GSM dual-band PA module has recently been announced [1]. This device achieves a 32-dBm output power and a 48% power-added efficiency (PAE) at a 3.4-V supply voltage and at a 1.8-GHz operating frequency.

Manuscript received April 5, 2002; revised August 7, 2002.

F. Carrara, T. Biondi, and G. Palmisano are with the Dipartimento Elettrico Elettronico e Sistemistico, Facoltà di Ingegneria, Università degli Studi di Catania, 95125 Catania, Italy (e-mail: fcarrara@deed.unict.it, fcarrara@dees.unict.it; tbiondi@dees.unict.it; gpalmisano@dees.unict.it).

A. Scuderi is with the STMicroelectronics Catania, 95121 Catania, Italy (e-mail: antonino.scuderi@st.com).

Digital Object Identifier 10.1109/TMTT.2002.805189

DCS-band performance parameters of commercial PAs are listed in Table I.[1] All the referenced amplifiers are based on III–V semiconductor technology. None of them is able to provide a higher than 2-W output power while operating under a lower than 3-V supply voltage. Moreover, PAE values rarely exceed 50% and power gains are typically lower than 30 dB. Therefore, most of the listed devices require an additional prepower amplifier (PPA), which further limits efficiency and increases the complexity of the overall transmitter.

This paper discusses the design and performance of a three-stage monolithic PA for 1.8-GHz wireless communications. The chip was fabricated using a low-cost silicon bipolar process [12]. Under a 2.7-V supply voltage, the amplifier delivers a 34-dBm output power with 57% PAE and 33-dB gain [13]. Measurements show that competitive performance with existing GaAs products can be obtained by using a silicon bipolar technology.

The effect of the emitter distributed resistance on the dc characteristics of long-emitter bipolar transistors is discussed in Section II. An analytical model for medium current levels is then derived and experimentally validated. The development and characterization of the unit power cell employed for the circuit's implementation is described in Section III. Finally, the design of the three-stage PA and its measured performance are presented in Sections IV and V, respectively.

II. DC Current Capability Degradation

In the design of integrated PAs, watt-range power levels are usually obtained by adding several unit cells in parallel, whose output power is summed up on a common collector node. For very high power levels, this technique is subject to severe limitations because outer devices remain less biased compared to inner ones due to the voltage drop across metal interconnections. As a consequence, the effective available emitter area is reduced to a fraction of the geometric one and diminishes as the number of parallel cells increases. Moreover, even with a moderate number of cells, the problem of parasitics due to interconnections still remains, leading to degradation in both input and output matching conditions.

On the other hand, the output power required can be achieved by lengthening the emitter fingers of the transistors, thus reducing the number of parallel cells and, hence, the voltage drop across the interconnections. However, excessively long transistors may suffer from current capability degradation as well, which is caused by the voltage drop across the distributed resistance of the emitter finger. Experimental results show

[1]Online product technical data is available through manufacturer websites.

TABLE I
DCS-BAND PERFORMANCE OF COMMERCIAL PAS

	Technology	V_{CC} [V]	P_{out} [dBm]	PAE [%]	Gain [dB]
Alpha AP134-501	InGaP HBT	3.2	32.5	50	27
Anadigics AWT6107	InGaP HBT	3.5	31.5	50	24
Motorola MRFIC1859	GaAs MESFET	3.6	34	43	29
EiC ECM007	InGaP HBT	3.5	32.5	50	30
Philips CGY2014TT	GaAs PHEMT	3.5	32.5	40	30
Raytheon RMPA1955-99	GaAs HBT	3.2	32.5	50	27
RF Micro Devices RF3108	GaAs HBT	3.5	33	52	27
Ericsson PBL 403 05	GaAs MESFET	3.2	31.7	41	23

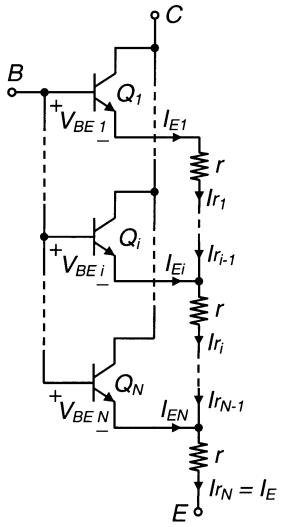

Fig. 1. N-section discretization of a bipolar transistor with distributed emitter resistance.

that in very-long emitter transistors this phenomenon becomes appreciable even at current levels well below the onset of high injection.

In order to find a good compromise between emitter length and cell number for the layout of the power transistor, the effect of the emitter distributed resistance on the transistor's dc characteristics was investigated. An analytical model was then derived to estimate the above degradation for medium injection levels.

A. Analytical Model

The current distribution along the transistor can be analyzed by dividing the device into N sections of equal length, as shown in Fig. 1. The emitter resistance of each section can be calculated as $r = R_E/N$, where R_E is the resistance of the whole emitter metal finger (metal sheet resistance times number of squares). Base and collector metal resistances are omitted because their effect on the current distribution is negligible.

Assuming that high injection effects can be neglected as well, the emitter current in each section follows the exponential law

$$\begin{aligned} I_{E_i} &\cong I_{ES_i} \cdot \exp\left(\frac{V_{BE_i}}{V_T}\right) \\ &= \frac{I_{ES}}{N} \cdot \exp\left(\frac{V_{BE_i}}{V_T}\right), \qquad i = 1, \ldots, N \end{aligned} \tag{1}$$

where I_{ES_i} and I_{ES} are the saturation currents of the ith section and the whole device, respectively.

The Kirchhoff law for the ith emitter node in Fig. 1 gives the current flowing through the ith section as

$$\begin{aligned} I_{r_i} &= I_{r_{i-1}} + I_{E_i} \\ &= I_{r_{i-1}} + \frac{I_{ES}}{N} \cdot \exp\left(\frac{V_{\mathrm{BE}}}{V_T}\right) \cdot \prod_{k=i}^{N} \exp\left(-\frac{R_E \cdot I_{r_k}}{N \cdot V_T}\right) \\ &= I_{r_{i-1}} + \frac{I_E^*}{N} \cdot \prod_{k=i}^{N} \exp\left(-\frac{R_E \cdot I_{r_k}}{N \cdot V_T}\right), \qquad i = 1, \ldots, N \end{aligned} \tag{2}$$

where I_E^* is the ideal emitter current in the case of zero degradation effects, i.e., $R_E = 0$

$$I_E^* \cong I_{ES} \cdot \exp\left(\frac{V_{\mathrm{BE}}}{V_T}\right). \tag{3}$$

A set of N equations with N unknowns is provided by (2) for $i = 1, \ldots, N$, whose solution gives the *degradation factor* (DF). This can be defined as the ratio of the actual emitter current I_E to the ideal emitter current I_E^*

$$\mathrm{DF} = \frac{I_E}{I_E^*}. \tag{4}$$

We can also define a *percentage of degradation*

$$\Delta A\% = 100 \cdot (1 - \mathrm{DF}) \tag{5}$$

that can be thought of as the percentage of emitter area remaining unused due to the voltage drop across the metal finger.

As N approaches infinity, approximations can be applied to the exponential term in (2) to linearize the set of equations. After manipulations and an iterative solution [14], DF and $\Delta A\%$ can be approximated, with little error, by the following simple first-order expressions:

$$\mathrm{DF} \cong 1 - \frac{\xi}{3} \quad \Delta A\% \cong 100 \cdot \frac{\xi}{3} \tag{6}$$

where

$$\xi = \frac{R_E \cdot I_E}{V_T}. \tag{7}$$

The first-order approximations provided by (6) hold for ξ values not exceeding the range $[0, 1]$, which is usually well met.

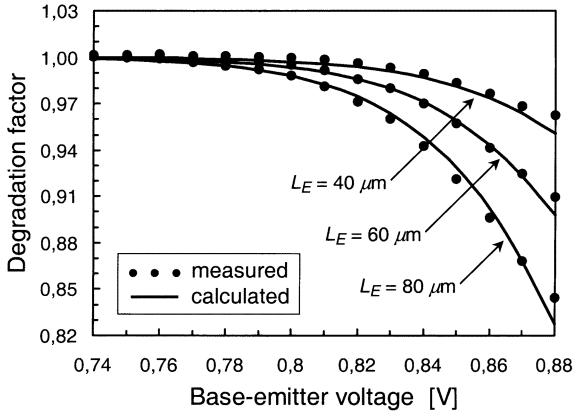

Fig. 2. Calculated and measured degradation factor as a function of the base–emitter voltage (the 10-μm transistor is taken as a reference for calculations).

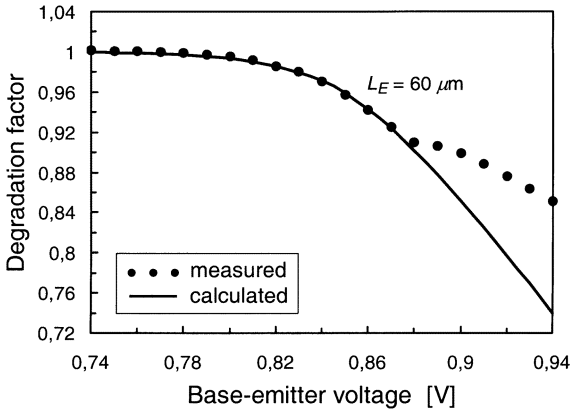

Fig. 3. High injection effects on the degradation factor.

Equation (6) is consistent with the analysis carried out in [15] by solving a differential equation.

B. Experimental Validation

To validate the analytical model, DF variation with emitter resistance was experimentally evaluated. To this purpose, transistors with a fixed emitter width and different emitter lengths were integrated for on-wafer measurements. The emitter width for all transistors was set to 0.8 μm, whereas the emitter length was varied from 10 to 80 μm. DC measurements were carried out by using a Cascade Microtech Prober and a semiconductor parameter analyzer. The emitter current was measured with a swept base–emitter voltage.

Of course, the ideal emitter current I_E^* is not available and DF values cannot be derived from single-device measurements. A comparison between analytical and experimental results is only possible in terms of DF ratios, which can be calculated as ratios of emitter current densities. In fact, from (4),

$$\frac{\mathrm{DF}_1}{\mathrm{DF}_0} = \frac{I_{E_1}}{I_{E_0}} \cdot \frac{I_{E_0}^*}{I_{E_1}^*} = \frac{I_{E_1}}{I_{E_0}} \cdot \frac{A_{E_0}}{A_{E_1}} = \frac{J_{E_1}}{J_{E_0}} \tag{8}$$

where subscripts 1 and 0 refer to the transistor under test and to a reference transistor, respectively. If the reference device is small enough to allow negligible degradation to be assumed (i.e., $\mathrm{DF}_0 = 1$), then (8) provides an easy way to evaluate the DF for the device-under-test.

A comparison between the calculated and measured data is shown in Fig. 2. The degradation factor of three transistors with emitter lengths of 40, 60, and 80 μm was calculated by using (8) and taking the 10-μm transistor as a reference. Modeled data show errors below 2% over the entire bias range, which confirms the accuracy of (6).

The same comparison is repeated in Fig. 3 for only the 60-μm device, but over a wider bias range. It is apparent from the curves displayed that (6) is not adequate to describe the phenomenon for high V_{BE} values, i.e., when the device is driven into the high current region. Actually, (1) and (3) are valid only below the forward knee current of the transistor. Therefore, the same limitation affects (6).

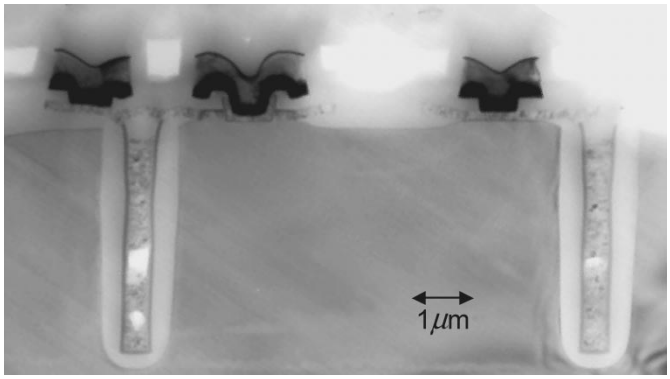

Fig. 4. HSB3 process TEM cross section.

III. Power Transistor Design

The preliminary steps of our study focused on the development of a unit power transistor to be used as a basic cell for the implementation of a three-stage PA. Both layout and technology arrangements were considered so as to optimize the power capability of the device. Load–pull measurements were carried out to compare different transistor solutions.

A. Silicon Bipolar Technology

The devices were fabricated on a 46-GHz f_T double-poly 0.8-μm self-aligned-emitter silicon bipolar process (HSB3) by STMicroelectronics, Catania, Italy. It is a low-cost technology, which requires only 17 mask steps. It provides oxide trench isolation, three metal layers, poly resistors, and metal–insulator–metal (MIM) capacitors with 0.7-fF/μm^2. On-chip spiral inductors are also available (3-μm–thick AlSiCu third metal layer) with Q values up to ten at 2 GHz and resonant frequencies above 15 GHz. Fig. 4 shows a TEM cross section of a transistor with a 0.8-μm emitter mask size.

B. Emitter Layout

As a first step, the effect of the emitter layout on the transistor power performance was investigated. To this end, two different power transistors were fabricated and tested, one with the standard continuous narrow strip (0.8 μm) emitter and the other with a spot emitter. Mask-level spot size was set to 0.8 μm$\times$ 2 μm. Harmonic load–pull measurements

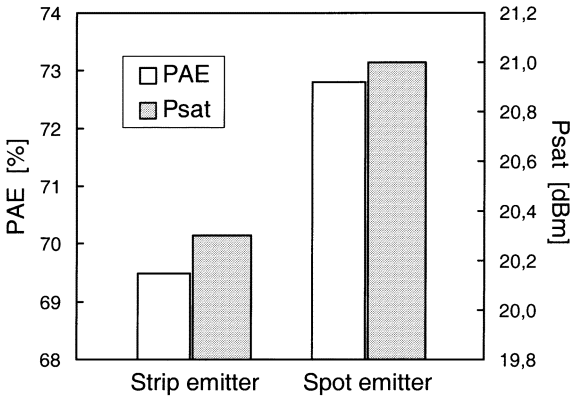

Fig. 5. Performance comparison between strip-emitter and spot-emitter transistors.

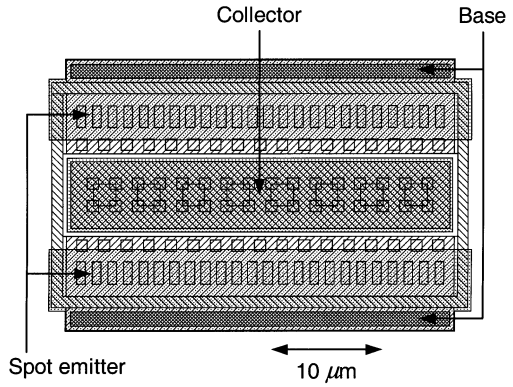

Fig. 6. Layout of the optimized unit power cell.

were performed on the two test devices under a 2.7-V supply voltage and a 1.8-GHz operating frequency using a single-tone continuous-wave (CW) input. Harmonic load impedances were tuned for maximum PAE, i.e., an open and a short circuit were provided at the second and third harmonic, respectively.

According to the performance comparison in Fig. 5, the spot emitter device was chosen for the PA design because it exhibited both higher PAE and saturated output power. The spot-transistor layout is shown in Fig. 6. Higher metal layers and stacked vias were exploited for better current draining.

The analytical model derived in Section II was considered to allow a proper emitter length to be set. A maximum tolerable degradation of 5% was assumed as a design target. Given a metal strip resistivity of 20 mΩ/square, a metal width of 5.5 μm, and an average current of 10 mA for each emitter finger, a maximum finger length of 36 μm was allowed according to (6), i.e., 48 emitter spots in all.

It is worth mentioning that a great improvement in DF is achieved when the emitter current is drained from both sides of the transistor. In this case, the percentage of degradation is reduced *by a factor of 4* since both R_E and I_E in (7) are halved.

C. Collector Dose and Thickness

At the second step, the 48-spot power cell was used as the reference device to test the effect of both the collector thickness and doping concentration on transistor performance. Four process splits were carried out, as shown in Table II. For comparison purposes, the results of dc, S-parameter, and harmonic load–pull measurements are summarized in Table III.

TABLE II
PROCESS SPLITS

	Epi-layer thickness [μm]	SIC dose
Lot A	1.2 (standard)	extra light
Lot B	1.2	light
Lot C	0.8	light
Lot D	0.8	standard

The best efficiency was achieved by reducing the epilayer thickness to 0.8 μm and using a standard dose for the selective implanted collector ($BV_{CEO} = 3.4$ V, $BV_{CES} = 14$ V). $P_{\rm out}$ and PAE performance was measured by the above-mentioned harmonic load–pull setup. A record 83% PAE and a 20.4-dBm saturated CW output power were achieved at a 1.8-GHz operating frequency and a 2.7-V supply voltage, as shown in Fig. 7. The small-signal power gain was 18 dB. A very good PAE of 75% was also obtained with a supply voltage as low as 1.8 V. The Gummel plot and the f_T characteristics of the optimized unit device are shown in Figs. 8 and 9, respectively.

IV. PA DESIGN

The optimized unit power cell was employed in the implementation of a monolithic PA for 1.8-GHz constant-envelope applications. Fig. 10 shows a simplified schematic of the amplifier. The circuit is composed of three stages (T1–T3). Based on load–pull measurements, a two-cell transistor was used for the first stage, an eight-cell transistor for the second, and a 32-cell one for the third.

As is well known, linearity is not a critical aspect in constant-envelope modulation schemes such as Gaussian minimum shift keying (GMSK), which is used in GSM and DCS systems. Indeed, information is conveyed in the phase of the modulated signal whose amplitude is kept constant. This allows PAs to be operated in nonlinear high-efficiency classes. PAE can be optimized by properly loading the power stage at both the fundamental and harmonic frequencies with multiresonant networks. The goal of such harmonic tuning is to shape the collector waveforms to let the collector current flow when the collector voltage is low and vice versa, thus minimizing transistor power consumption. According to load–pull measurements, optimum power performance can be achieved by providing an open and a short circuit at the second and third harmonic, respectively (i.e., dual-class-F operation [16]). Regrettably, the implementation of a class-F-like multiresonant load is quite difficult at RF frequencies because of package parasitics and process tolerances. Therefore, a single-resonator solution was selected for the off-chip output matching network (only a second harmonic control was performed). Under such conditions, nonlinear circuit simulations showed that best power performance can be achieved when a high reactive impedance tending toward an open circuit is provided for the harmonics of the fundamental frequency, i.e., by using a series-resonant load. Such a load leads to a pulsed collector voltage and a sinusoidal collector current

TABLE III
TYPICAL PERFORMANCE PARAMETERS

	Lot A	Lot B	Lot C	Lot D	Test conditions
$h_{FE\,max}$	127	156	155	169	V_{CB} = 0 V
V_{AF} [V]	59	49	41	28	V_{BE} = 0.75 V
BV_{CEO} [V]	6.4	5.3	4.3	3.4	I_B = 0 A
$f_{T\,max}$ [GHz]	22	28	32	43	V_{CB} = 0 V
f_{max} [GHz]	29	30	30	33	V_{CB} = 0 V
MAG [dB]	8	13	15	17	f = 5 GHz, V_{BE} = 0.9 V, V_{CB} = 0 V
P_{sat} [dBm]	17.7	17.8	20.3	20.4	f = 1.8 GHz, V_{CC} = 2.7 V, CW test
PAE_{max} [%]	69	71	82	83	f = 1.8 GHz, V_{CC} = 2.7 V, CW test
P_{sat} [dBm]	-	-	-	17.3	f = 1.8 GHz, V_{CC} = 1.8 V, CW test
PAE_{max} [%]	-	-	-	75	f = 1.8 GHz, V_{CC} = 1.8 V, CW test

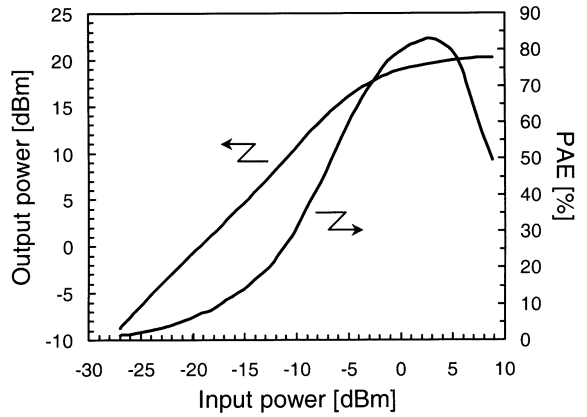

Fig. 7. Output power and PAE versus input power for the optimized power cell ($V_{CC} = 2.7$ V, $f = 1.8$ GHz, harmonic load–pull CW test).

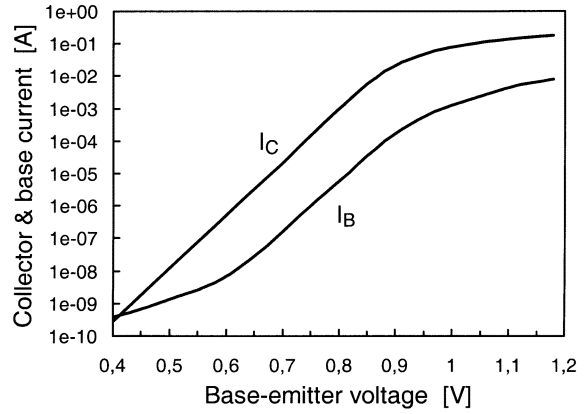

Fig. 8. Gummel plot of the optimized power cell ($V_{CB} = 0$).

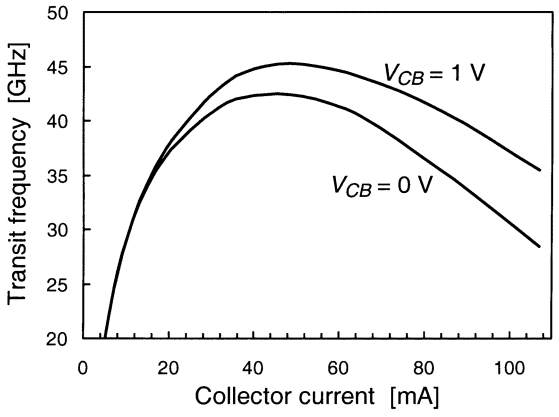

Fig. 9. Transit frequency versus collector current for the optimized power cell.

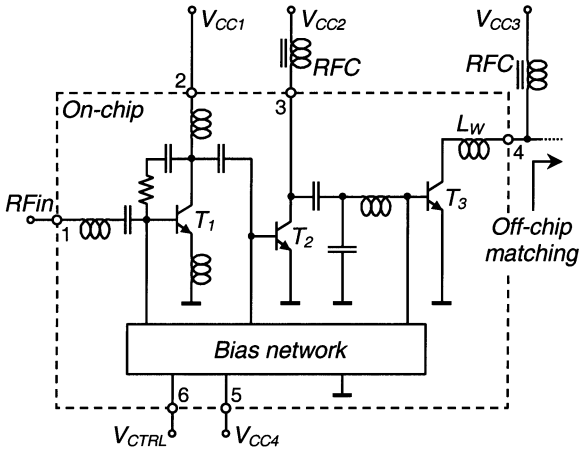

Fig. 10. Simplified schematic of the three-stage PA.

(mixed-C mode [17] or class C-E [18]). Dual waveforms, i.e., a pulsed current and sinusoidal voltage, are generated by a parallel-resonant load. However, it produces a higher current peak, which leads to an increased voltage drop across the collector series resistance and, hence, a reduction in PAE.

Fig. 11 outlines the partially distributed transformation network that was used for off-chip output matching. Bond-wire inductance L_W was properly employed to implement a series-resonant load for the third stage. Both the second and third stages were biased through external pull-up inductors. As an alternative to RF chokes, printed circuit board (PCB) quarter-wave shorted stubs could be employed for better second harmonic suppression [18].

On-chip reactive networks provide interstage impedance matching, which was designed for maximum gain under large-signal conditions. The goal of maximum bandwidth was also considered for the interstage matching to compensate for device process tolerances. A bond-wire inductance and capacitor were used between the first and second stages, whereas two capacitors and a spiral inductor were employed between the second and third stages. To improve the inductor performance, a close honeycomb-patterned oxide trench was used, which broke up the buried layer below the metal spirals,

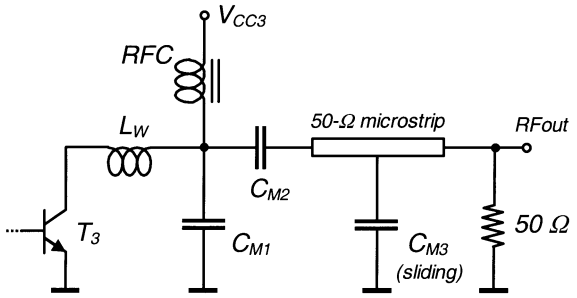

Fig. 11. Matching network at the PA output.

thus preventing eddy currents and inductance reduction. The integrated inductor achieved a Q value of nine at 1.8 GHz and a resonant frequency above 15 GHz. On-chip input matching was also implemented by means of two bond-wire inductances at the emitter and base of the first stage.

A bias circuit was included, which allows a power control function to be achieved by varying the base quiescent current of each stage through the external voltage $V_{\rm CTRL}$. In the design of the bias network, the goal of maximum PAE at reduced output power levels was taken into account. Since the last stage is the most power-consuming one, as $V_{\rm CTRL}$ decreases, a stronger base current reduction is imposed to the third stage compared to the first and second stages.

The circuit was simulated using the harmonic-balance method with Agilent ADS. An improved Gummel–Poon large-signal model was used to accurately describe the nonlinear behavior of transistors (ST-SPICE Gummel–Poon model by STMicroelectronics [19]). The standard model was properly modified to account for the Kirk effect, which affects bipolar junction transistor (BJT) performance under high-current low-voltage conditions. Extensive S-parameter measurements were carried out under various bias conditions to extract best-fitting nonlinear model parameters.

Minimization of the ground inductance is an important issue in the design of RF PAs since it greatly affects overall gain and PAE. To decrease such parasitics, both the second and third stages were provided with on-chip ground planes by using the third metal layer. Moreover, a solderable-pad package was selected for circuit assembly and a large number of down-bonding wires was used to connect the on-chip ground planes to the die pad (through-wafer vias not available in the process). Extensive electromagnetic simulations were performed for accurate estimation of ground inductances at the operating frequency and its harmonics. ADS Momentum was employed for two-dimensional (2-D) simulations of the ground planes, whereas Ansoft HFSS was used for three-dimensional (3-D) simulations of down-bonding wires. Ground inductances values below 0.1 nH were estimated.

V. Experimental Results

A die photograph of the fabricated amplifier is shown in Fig. 12. The chip size is 1.8 mm × 1.8 mm. Most of the die area is spent for the on-chip ground planes to minimize ground parasitic inductances. Measurements were performed on a 400-μm–thick FR4 substrate to conform to the low-cost

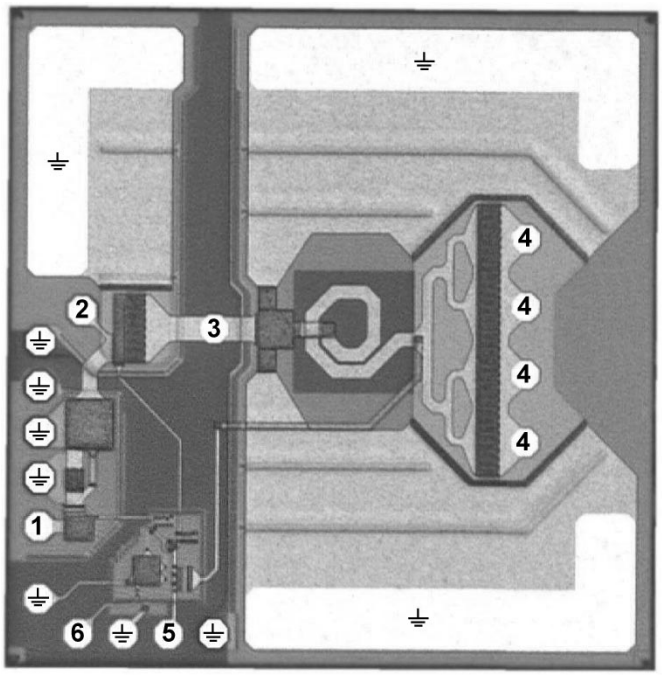

Fig. 12. Die photograph of the PA (see Fig. 10 for pin reference).

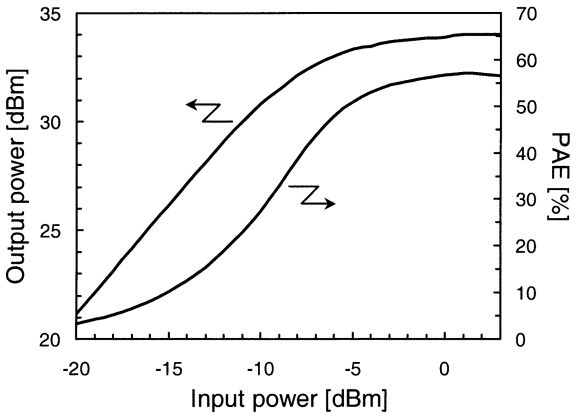

Fig. 13. Output power and PAE versus input power for the three-stage PA ($V_{CC} = 2.7$ V, $f = 1.8$ GHz, pulsed mode test).

production environment. The die was molded in a small 16-pin leadless plastic package providing an exposed bottom pad for RF grounding and heat dissipation. Package size is $4 \times 4 \times 0.9$ mm.

Fig. 13 shows the output power and PAE performance versus input power at 1.8 GHz. A 57% maximum PAE is achieved at a 34-dBm output power level while operating with a 2.7-V supply voltage. The second and third harmonics are 45 and 37 dB below the carrier, respectively. Only a very small input power is required to drive the PA since the device exhibits a 33-dB power gain under maximum PAE conditions, as well as a 41-dB small-signal gain. Despite such a high small-signal gain, no oscillation occurred since high substrate coupling rejection was provided by means of trench isolation and buried-layer grounding.

Fig. 14 shows the dependence of the output power and PAE on the operating frequency. It is worth mentioning that the gain variation over the entire DCS transmit window

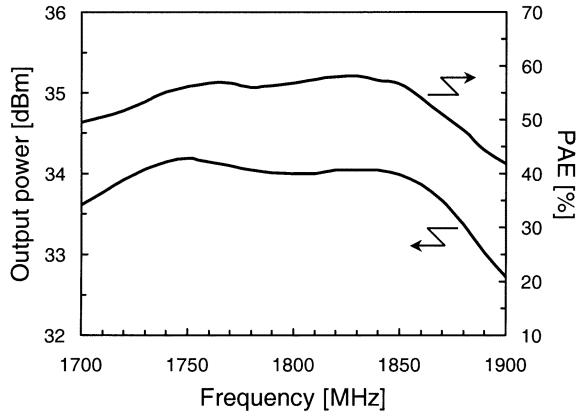

Fig. 14. Output power and PAE versus operating frequency ($V_{CC} = 2.7$ V, $P_{\rm in} = 1$ dBm).

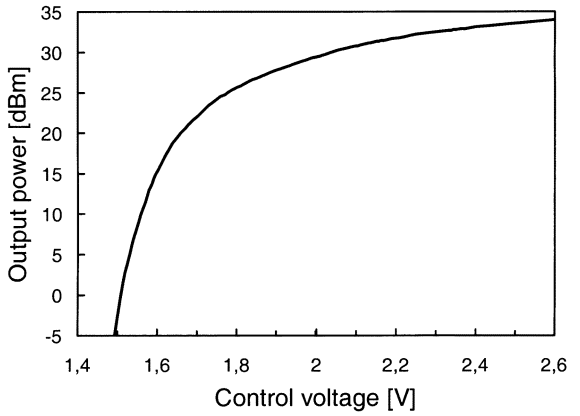

Fig. 15. Output power versus control voltage ($V_{CC} = 2.7$ V, $f = 1.8$ GHz, $P_{\rm in} = 1$ dBm).

(1710–1785 MHz) is less than 0.5 dB. This result derives from the use of bandwidth-optimized matching networks for process spread compensation.

Output power versus control voltage $V_{\rm CTRL}$ is shown in Fig. 15. By means of the bias network implemented, the power control function is successfully achieved.

VI. Conclusions

The potential of a high-performance low-cost silicon bipolar technology for high-efficiency low-voltage RF PAs has been explored. To this end, a unit power cell has been developed by optimizing the layout design, collector thickness, and doping level. An analytical model has been derived to provide an estimation of the current capability degradation due to the emitter finger distributed resistance. Comparison with measured data has shown very good agreement for current levels up to the forward knee current. On-wafer load–pull measurements have been performed on the developed power transistor, which showed an excellent PAE of 83% at 1.8 GHz. The optimized unit power cell has been employed to implement a 1.8-GHz three-stage monolithic PA. The device achieved a 57% PAE and 33-dB gain at a 34-dBm output power level while operating at 2.7 V. These results amount to the best power performance reported so far reported for a silicon bipolar device operating in the 1.8-GHz band under a supply voltage lower than 3 V.

This paper has demonstrated that silicon bipolar PAs can be considered as excellent candidates for low-voltage low-consumption transmitters in mobile handsets.

Acknowledgment

The authors would like to thank A. Castorina, STMicroelectronics, Catania, Italy, G. Privitera, STMicroelectronics, and G. Conti, STMicroelectronics, for their assistance with measurements.

References

[1] T. Johansson, P. Lundin, J. Engvall, D. Uggla, and U. Hagström, "A high efficiency, low cost silicon bipolar GSM dual-band PA module," *Microwave J.*, vol. 44, no. 12, pp. 60–70, Dec. 2001.

[2] S. L. Wong, H. Bhimnathwala, S. Luo, B. Halali, and S. Navid, "A 1 W 830 MHz monolithic BiCMOS power amplifier," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 1996, pp. 52–54.

[3] D. Su and W. McFarland, "A 2.5 V, 1 W monolithic CMOS RF power amplifier," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1997, pp. 189–192.

[4] S. Weber and G. Donig, "An integrated 2 GHz 500 mW bipolar amplifier," in *IEEE RFIC Symp. Dig.*, June 1997, pp. 139–142.

[5] I. Yoshida *et al.*, "A 3.6 V 4 W 0.2 cc Si power-MOS-amplifier module for GSM handset phones," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 1998, pp. 50–51.

[6] R. Parkhurst *et al.*, "Silicon bipolar 3 V power amplifier for GSM900/GSM1800 handsets," in *Proc. IEEE Bipolar/BiCMOS Technol. Meeting*, Sept. 1998, pp. 117–119.

[7] K.-C. Tsai and P. R. Gray, "A 1.9-GHz, 1-W CMOS class-E power amplifier for wireless communications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 962–970, July 1999.

[8] C. Fallesen and P. Asbeck, "A 1 W 0.35 μm CMOS power amplifier for GSM-1800 with 45% PAE," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2001, pp. 158–159.

[9] D. Heo, A. Sutono, E. Chen, Y. Suh, and J. Laskar, "A 1.9-GHz DECT CMOS power amplifier with fully integrated multilayer LTCC passives," *IEEE Microwave Wireless Comp. Lett.*, vol. 11, pp. 249–251, June 2001.

[10] W. Simburger, H.-D. Wohlmuth, P. Weger, and A. Heintz, "A monolithic transformer coupled 5-W silicon power amplifier with 59% PAE at 0.9 GHz," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1881–1892, Dec. 1999.

[11] W. Simbürger *et al.*, "A monolithic 2.5 V, 1 W silicon bipolar amplifier with 55% PAE at 1.9 GHz," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2000, pp. 853–856.

[12] F. Carrara, A. Scuderi, G. Tontodonato, and G. Palmisano, "A very high efficiency silicon bipolar transistor," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, Dec. 2001, pp. 883–886.

[13] F. Carrara, A. Castorina, A. Scuderi, and G. Palmisano, "High performance silicon bipolar power amplifier for 1.8 GHz applications," in *IEEE MTT-S Int. Microwave Symp.*, June 2002, pp. 1015–1018.

[14] F. Carrara, T. Biondi, A. Scuderi, and G. Palmisano, "Degradation of the DC current capability in long-emitter bipolar transistors," in *IEEE Int. Electron., Circuits, Syst. Conf.*, Sept. 2002, pp. 1195–1198.

[15] K. J. S. Cave and J. A. Barnes, "Optimum length of emitter stripes in 'comb' structure transistors," *IEEE Trans. Electron Devices*, vol. ED-12, pp. 84–85, Feb. 1965.

[16] F. H. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2007–2012, Nov. 1997.

[17] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*. New York: Wiley, 1980.

[18] F. J. O. Gonzalez, J. L. J. Martin, and A. A. López, "Effects of matching on RF power amplifier efficiency and output power," *Microwave J.*, vol. 41, no. 4, pp. 60–72, Apr. 1998.

[19] D. Celi, "BJT model equations," STMicroelectronics, Crolles, France, Oct. 1989.

Francesco Carrara (S'01) was born in Catania, Italy, in 1973. He received the Laurea degree in electronics engineering (*cum laude*) from the University of Catania, Catania, Italy, in 1999, and is currently working toward the Ph.D. degree in electronics and automation engineering at the University of Catania.

Since 1999, he has been with the Radio Frequency Advanced Design Group (RF-ADG), a joint research group supported by the University of Catania and STMicroelectronics, Catania, Italy, where he is involved in the design and development of RF PAs for third-generation mobile handsets. His current research interests include high-efficiency amplifier design, amplifier linearization techniques, and silicon bipolar devices for wireless communications.

Antonino Scuderi was born in Catania, Italy, in 1972. He received the Laurea degree in electronics engineering (*cum laude*) from the University of Catania, Catania, Italy, in 1997.

Since 1999, he has been with STMicroelectronics, Catania, Italy, where he is with the Radio Frequency Advanced Design Group (RF-ADG), a joint research group supported by the University of Catania and STMicroelectronics, Catania, Italy. He is currently engaged in the design and development of RF PAs for cellular handsets. His current research interests include high-efficiency amplifier design, PA overvoltage protection techniques, and silicon bipolar devices for wireless communications.

Tonio Biondi was born in Catania, Italy, in 1976. He received the Laurea degree in electronics engineering (*cum laude*) from the University of Catania, Catania, Italy, in 2000, and is currently working toward the Ph.D. degree in electronics and automation engineering at the University of Catania. In 2001, he attended the "Advanced Course on Microelectronics and Systems" at the Istituto Superiore per la Formazion di Eccellenza, Catania, Italy.

Since 2000, he has been with the Radio Frequency Advanced Design Group (RF-ADG), a joint research group supported by the University of Catania and STMicroelectronics, Catania, Italy, where he is involved in the characterization and modeling of active and passive silicon integrated components. During 2002, he was with the Integrated Circuit Characterization and Development Group, STMicroelectronics, Crolles, France, where he was involved with large-signal load–pull characterization and nonlinear modeling of high-efficiency RF power bipolar transistors. His current research interest lies in the characterization and modeling of active and passive silicon integrated devices for wireless communication systems.

Giuseppe Palmisano received the Laurea degree in electronics engineering from the University of Pavia, Pavia, Italy, in 1982.

From 1983 to 1991, he was a Researcher with the Department of Electronics, University of Pavia, where he was involved in CMOS and BiCMOS analog integrated-circuit design. In 1992, he was a Visiting Professor with the Universidad Autonoma Metropolitana (UAM), Mexico City, Mexico, where he taught a course on microelectronics. In 1993, he joined the Faculty of Engineering, University of Catania, Catania, Italy, as an Associate Professor. He is currently a Full Professor teaching microelectronics. Since 1999, he has led the Radio Frequency Advanced Design Group (RF-ADG), a joint research group supported by the University of Catania and STMicroelectronics, Catania, Italy. He has designed several innovative analog integrated circuits within the framework of national and European research projects and in collaboration with electronics industries. He has coauthored over 100 papers in international journals and conference proceedings and a book on current operational amplifiers. He holds several international patents. His current research interest lies in the design of RFICs for portable communications equipment.